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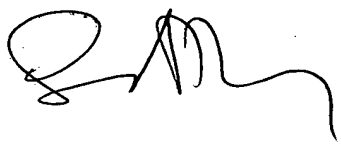

For and on behalf of RWS Group Ltd

The 1st day of March 2006

FEDERAL REPUBLIC OF GERMANY

[Eagle crest]

Priority Certificate

for the filing of a Patent Application

File Reference:	101 40 045.4
Filing date:	16 August 2001
Applicant/Proprietor:	Infineon Technologies AG, 81669 Munich/DE
Title:	IC chip having a protective structure
IPC:	H 01 L, H 05 K

The attached documents are a correct and accurate reproduction of the original submission for this Application.

Munich, 9 February 2006

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The President

pp

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Stark

Description

IC chip having a protective structure

The present invention relates to a semiconductor chip having a protective structure for protecting against a malfunction caused by irradiation, said chip being intended, in particular, for use in smart cards.

The function of integrated circuits in semiconductor chips may be adversely affected by electromagnetic or radioactive irradiation. The irradiation may generate free charge carriers in the semiconductor material, said charge carriers generating undesirable currents when potential differences are present. These currents give rise to a malfunction or at least a change in function in the integrated circuit. For applications relevant to security, semiconductor chips are therefore provided with protective structures which, for example, may be formed by shields on the top side of the chip. Shields of this type may be formed by protective layers comprising an electrically insulating material which is impermeable to radiation; instead, provision may also be made of suitably patterned electrical conductors which, apart from shielding, also make it possible to electronically detect irradiation. Various technical realizations of protective structures comprising sensors are known, said sensors being used to detect irradiation of a semiconductor chip. Sensors of this type are arranged in the vicinity of those regions of the integrated circuit which are adversely affected by irradiation. However, it has been shown that the irradiation may be focused in such a manner or, using masks, may be directed toward particular parts of the circuit in such a manner that although functional disturbances are produced, none of the sensors provided responds. This problem arises, in particular, in

semiconductor memory elements such as, for example, in EEPROMs.

An object of the present invention is to specify an IC chip having a protective structure, which is sufficiently effective against external irradiation and, in particular, also protects against focused radiation.

This object is achieved by means of the IC chip having the features of claim 1, claim 3, claim 6 or claim 9. Refinements emerge from the dependent claims.

The IC chip according to the invention indicates possibilities regarding the manner in which the protective structure is distributed over the semiconductor chip in such a way that it is not possible, by means of irradiation, to trigger a malfunction in a region of the integrated circuit without the protective structure also being affected by the irradiation in a detectable manner.

A first of these possibilities, which is advantageous, in particular, in connection with semiconductor memory components, provides for at least one electrical conductor (which is present in the integrated circuit) or at least one electrically conductive connection to be provided, in a redundant manner, with a further electrical conductor or with an identical connection, which is respectively in the form of a doped region in the semiconductor material. The effect achieved by this is that any external electromagnetic or radioactive irradiation affecting an electrical conductor of the integrated circuit also affects the associated doped region and generates free charge carriers there which give rise to a flow of current during operation of the circuit. This flow of current may be detected by a connected circuit.

This possibility is particularly advantageous in connection with the data lines of a memory component. The doped regions may be aligned under the data line, in particular the bit lines. Since the data lines form a dense grid on the top side of the IC chip, any irradiation will generate charge carriers at least in one doped region running parallel to these data lines, said charge carriers resulting in an unusually high flow of current in the data line in question. External irradiation at an arbitrary location on the top side of the IC chip may be detected in this manner.

An alternative protection mechanism for an IC chip provided with a memory, in particular with an EEPROM, uses the transmission of additional data (which is carried out anyway) as check digits or a code number in order to detect external irradiation. That is to say, when reading memory cells, redundant bits are concomitantly transmitted for the purpose of error correction. This additional information is used to check whether the data transmitted on the data lines are corrupted.

The further data lines for these check digits or code numbers are arranged between the data lines which are intended for transmitting the actual information. An algorithm, in which the further data are selected to be as complementary as possible to the data to be transmitted, is provided for correcting a defective data transmission, if necessary, on the basis of the redundant bits transmitted on the further data lines. The check bit "F" of the number 15 is, for example, formed in a hexadecimal number system for a stored value "00". Selecting the further data (which are provided for the purpose of correction) in this manner achieves the effect that external irradiation of the IC chip changes the information carried on the data lines

all in the same direction. By way of example, all bits are changed to the logic value "1" irrespective of whether a "0" or a "1" was initially transmitted.

It emerges from the particular selection of the check digits or code numbers formed that, when the data are changed by irradiation, the check bits, with the exception of an insignificantly small number of special cases, do not match the transmitted information. The correction algorithm provided will therefore ascertain corruption of the transmitted data which is so extensive that corruption of the data by external irradiation may be assumed and appropriate countermeasures may possibly be initiated. Since the check bits are calculated in an unambiguously determined manner from the data to be transmitted, it is virtually no longer possible in this refinement of the IC chip to prevent triggering of a protection function provided in the circuit by changing the further data in a suitable manner together with the transmitted information. That part of the circuit, in which the correction algorithm is implemented, is preferably configured in such a manner that, in the event of a change in function caused by irradiation or corruption of the transmitted data, a signal is output such as is also emitted by a protection circuit provided with a sensor.

A further exemplary embodiment provides for a shield, which is present on the chip anyway and is formed from patterned electrical conductors, to be modified to the effect that external electromagnetic or radioactive irradiation may be detected. The shield is usually present in a topmost metallization plane of the chip. If a plurality of metallization planes are provided for the electrical interconnection, they are isolated from one another by intermetal dielectrics. The latter are usually oxide layers, for example silicon dioxide. A

passivation or protective layer for protecting against external stress may be provided on the top side of the topmost metallization plane, that is to say that metallization plane which is furthest away from the semiconductor material of the chip. A passivation of this type usually likewise comprises electrically insulating material.

At least one of the layers above or below the topmost metallization plane or in the interspaces between the patterned electrical conductors of this metallization plane is a particular dielectric material, which, upon the action of external electromagnetic or radioactive irradiation, undergoes a change in its relative permittivity to an extent which is relevant in terms of circuitry. This may be effected, in particular, by a change in the number of free charge carriers present in the material. The relative permittivity always changes in such a manner that the change can be detected by means of circuitry, for example by determining the change in the electrical capacitance between the electrical conductors which are embedded in said material or adjoin said material.

A further possibility is to provide a material between the electrical conductors, the electrical resistance of said material, in the event of external irradiation, decreasing in such a manner that a certain electrical conductivity between two electrical conductors (insulated from one another beforehand) can be detected through this material or a conductive connection, a short circuit in the extreme case, is even produced between said conductors.

The features of the above-described exemplary embodiments may be combined with one another in a selection which is in principle arbitrary, it being possible for this to result in a considerable

improvement in the protective action. In particular, a combination of all the specified means may be preferred in order to protect memory chips against irradiation.

A more precise description of exemplary embodiments of the IC chips follows with reference to the appended figures 1 to 3.
Figure 1 shows a diagrammatic cross section through an IC chip having redundant conductive connections.
Figure 2 shows a diagrammatic plan view of a memory component having distributed test lines.
Figure 3 shows a diagrammatic cross section through an IC chip having connecting structures comprising dielectric material of radiation-dependent electrical resistance.

Figure 1 illustrates a first exemplary embodiment of an IC chip, the internal structure of which may in principle be arbitrary and in this case is represented by a semiconductor body or by a substrate 1. Electrical conductors 2 which are indicated here by the cross sections of bit lines or word lines are situated on said substrate. Strip-type doped regions 3 which are arranged parallel to said conductors 2 are situated under the latter in the semiconductor material. Mobile charge carriers in the material are generated in the doped regions 3 by means of particular external electromagnetic or radioactive irradiation operations. If an electric current flows in the conductors 2, the current intensity is increased, in the event of external irradiation, by the free charge carriers occurring in the doped regions 3. This increased current intensity may be detected and is an indication of the fact that the functioning of the circuit is changed by external irradiation.

The doped regions 3 do not need to be connected to the conductors in the manner illustrated in figure 1. A

spacing may be present between the conductors 2 and the doped regions 3, it being possible for said spacing to even be bridged by an electrically insulating material. The doped regions 3 may also be laterally offset with respect to the conductors, with the result that, in the example illustrated in figure 1, the doped regions may also be arranged between the regions of the substrate which are provided with the conductors 2. The doped regions 3 do not need to be present over the entire length of the conductors 2. It suffices if the doped regions are present in a section which is possibly exposed to irradiation or a plurality of sections of this type and are arranged in such a manner that they are likewise included by the irradiation. The doped regions are preferably provided with separate electrical connections to the circuit provided, so that, on the one hand, it is possible to dispense with a low-resistance conductive connection to the conductors 2 and, on the other hand, it is possible to detect more efficiently a current occurring in the doped regions in the event of electromagnetic or radioactive irradiation.

Figure 2 illustrates the arrangement of data lines and further data lines of an IC memory chip 10. The number of data lines and further data lines is arbitrary; in particular, only one data line and/or only one further data line need(s) to be present. The further data lines are arranged in the vicinity of the data lines or are arranged between the data lines or interlaced therewith, so that it is not possible, or it is at best possible with considerable outlay, to change the data carried on the data lines (in this case: bit lines) separately from the data carried on the further data lines (in this case: test lines) and, separately therefrom, likewise to change the check bits carried on the further data lines so that they match the changed data. The strips depicted in figure 2 may, for example,

be the bit lines of an EEPROM. The bit lines BL0, BL1, BL2, BL3, BL4, BL5, BL6 and BL7 are provided as data lines for transmitting information. The test lines PL0, PL1, PL2 and PL3 are arranged between the bit lines in such a manner that it is not possible, or it is at best possible with considerable outlay, to change the data transmitted on the bit lines without also changing the further data on the test lines. Any change to the data by external electromagnetic or radioactive irradiation thus leads to the situation where the (randomly changed) check bits, check digits or code numbers for data correction which have actually been transmitted allow the conclusion to be drawn of a change in the (randomly changed) information transmitted on the data lines which is so considerable that an attempt at manipulation by external irradiation may be assumed and appropriate countermeasures may possibly be initiated.

Figure 3 illustrates a diagrammatic cross section of a further exemplary embodiment, in which the IC chip is provided on the top side with a conductor structure having radiation-dependent electrical resistance. A semiconductor body or substrate 1 is shown again here, the more precise configuration of which is in principle arbitrary. Conductors 4, 5 (between which a dielectric material is arranged as connection 6) are present here on the top side of the substrate, in particular on the top side of the metallization planes and intermetal dielectrics (arranged above the actual semiconductor body) for the electrical interconnection. In one preferred refinement, said material is selected in such a manner that its relative permittivity changes in the event of external electromagnetic or radioactive irradiation or its electrical resistance decreases in the event of irradiation of this type. The conductors 4, 5 may, in particular, be parts of a patterned shield.

In the event of external irradiation, it is possible to detect the accompanying change in capacitance between the electrical conductors 4, 5 and/or an increase in the electrical conductivity of the connection 6 present between the latter. If the resistance of the material of the connection 6 has decreased by at least a particular predetermined value, it may be assumed that the integrated circuit is being manipulated by external irradiation. In this case, appropriate countermeasures may be initiated as required.

Patent Claims

1. An IC chip having a protective structure for protecting against a malfunction caused by irradiation, in which
there is an integrated circuit, which has at least one electrical conductor (2),
there is at least one region in which external electromagnetic or radioactive irradiation can give rise to a change in function, and
there is a protective structure for detecting said change in function,
characterized in that
the electrical conductor (2) is supplemented by a further electrical conductor, which is in the form of a region (3), in which external electromagnetic or radioactive irradiation generates free charge carriers which give rise to a flow of current during operation of the circuit, and
the protective structure detects the occurrence of this flow of current.

2. The IC chip as claimed in claim 1, in which
the integrated circuit is part of a memory,
there are a plurality of electrically conductive connections (2) which are provided as data lines and comprise interconnects, and
a respective identical connection is a doped region, which is formed in semiconductor material and is arranged parallel to a respective interconnect.

3. An IC chip
having a memory,
having at least one data line (BL0, BL1, BL2, BL3, BL4, BL5, BL6, BL7) and
having at least one further data line (PL0, PL1, PL2, PL3), which is intended for transmitting further data

which are used to check whether the data transmitted on the at least one data line are corrupted,
characterized in that
the at least one further data line is arranged in or on the chip in the vicinity of the at least one data line or further data lines are arranged between the data lines or are interlaced therewith, with the result that external electromagnetic or radioactive irradiation of the data line for the purpose of changing the transmitted data also affects the at least one further data line to an extent which suffices to change the transmitted further data.

4. The IC chip as claimed in claim 3, in which
the at least one further data line is intended for transmitting a check digit, a check number or code number, which results, in an unambiguously determined manner, from the transmitted data.

5. The IC chip as claimed in one of claims 2 to 4, in which
the memory is an EEPROM.

6. An IC chip
having semiconductor material and
having one or more metallization planes which are isolated from one another and/or covered by a dielectric,
characterized in that
a material, the relative permittivity of which changes to an extent which is relevant in terms of circuitry under the influence of external electromagnetic or radioactive irradiation, is selected as the dielectric at least above or below a particular metallization plane or within a layer formed by said metallization plane.

7. The IC chip as claimed in claim 6, in which

there are two metallization planes between which said dielectric is present, and
an integrated circuit is provided for detecting a change in the electrical capacitance between said metallization planes.

8. The IC chip as claimed in claim 6, in which
a metallization plane is patterned in parts which are electrically insulated from one another by means of said dielectric, and
an integrated circuit is provided for detecting a change in the electrical capacitance between said parts.

9. An IC chip
having a structure of electrical conductors (4, 5) between which a connection (6) comprising a material, the electrical resistance of which decreases under the action of external electromagnetic or radioactive irradiation, is arranged in such a manner that, in the case of irradiation of this type, the decrease in the electrical resistance of the connection is detected by a circuit provided for this purpose.

10. The IC chip as claimed in claim 1 or 2 and/or as claimed in one of claims 3 to 5 and/or as claimed in one of claims 6 to 8 and/or as claimed in claim 9,
which is intended for use in a smart card or for forming a chip module.

P2001,0593 DE E

Abstract

IC chip having a protective structure

The protective structure is distributed over the semiconductor chip (1) in such a manner that it is not possible to trigger a malfunction in the circuit by means of irradiation without the protective structure also being affected by the irradiation. To this end, redundant conductors (3) are provided or connections having radiation-dependent conductivity or dielectric constant are provided or the test lines of a memory are arranged between the bit lines.

Figure 1

List of reference symbols

1	Substrate
2	Conductor
3	Doped region
4	Conductor
5	Conductor
6	Connection
10	IC memory chip
BL0	Bit line
BL1	Bit line
BL2	Bit line
BL3	Bit line
BL4	Bit line
BL5	Bit line
BL6	Bit line
BL7	Bit line
PL0	Test line
PL1	Test line
PL2	Test line
PL3	Test line

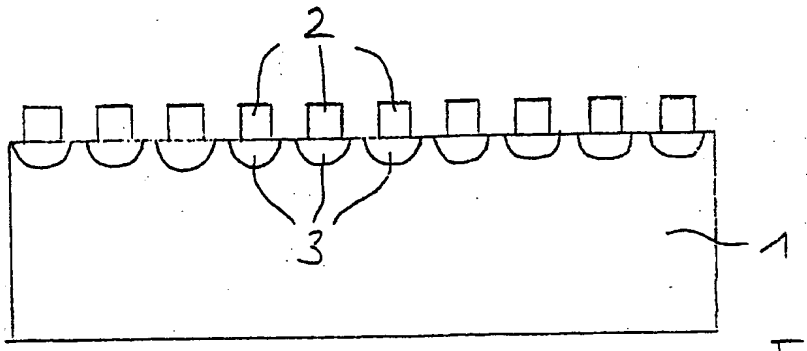

Fig 1

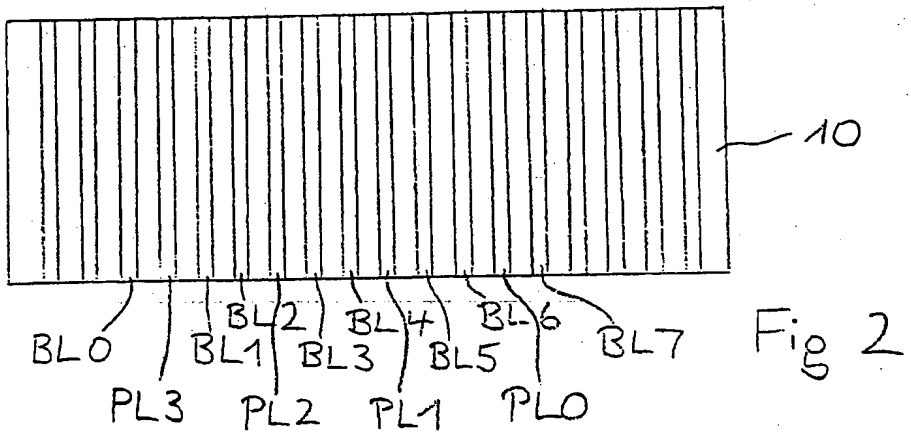

Fig 2

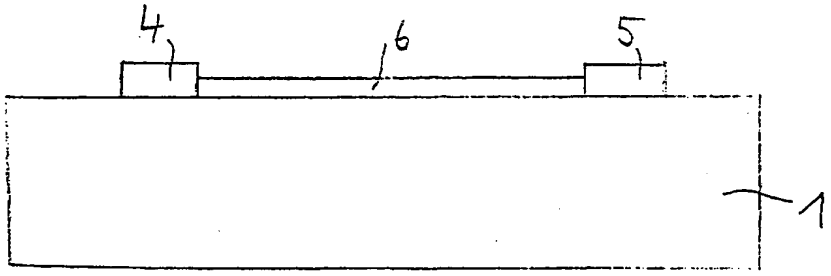

Fig 3